UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,432	08/01/2003	Vincent J. Zimmer	INTEL/16808	4540

34431 7590 06/14/2006

HANLEY, FLIGHT & ZIMMERMAN, LLC
20 N. WACKER DRIVE
SUITE 4220
CHICAGO, IL 60606

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,432	ZIMMER ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on April 25, 2006. This amendment has been entered and carefully considered. Claims 1-45 are again presented for examination.

2. Applicant's arguments filed on April 25, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-6, 8-13, 15-17, 19-21, 23-28, 30-32, 34-36, 38-43 and 45 are rejected under 35 U.S.C. 102(a) as being anticipated by Poisner et al. (USPN: 2002/0199093) hereinafter, Poisner.

4. Claims 1-2, 4-6, 8-13, 15-17, 19-21, 23-28, 30-32, 34-36, 38-43 and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Poisner.

The applied reference has a common assignee and inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, Poisner teaches a method of migrating storage from a temporary memory location in a temporary memory (i.e. CPU's cache memory; embedded in CPU 100 in Fig. 1A-1B) to a main memory location in a main memory (i.e. the external/separate RAM for BIOS processing, the main memory 102 in Fig. 1A-1B), the method comprising: copying content from the temporary memory location to the main memory location; calculating a migration factor between the temporary memory location and the main memory location; and modifying a value in the main memory that identifies the temporary memory location to identify the main memory location (e.g. see Paragraph [0028] and Figs. 1-2).

As per claim 2, Poisner teaches the claimed invention as described above and furthermore, Poisner teaches that the content comprises stack data (e.g. see Paragraph [0011], lines 1-4).

As per claim 4, Poisner teaches the claimed invention as described above and furthermore, Poisner teaches that the temporary memory comprises a cache memory

(i.e. CPU's cache memory; embedded in CPU 100 in Fig. 1A-1B) (e.g. see Paragraph [0005] and Figs. 1A-1B).

As per claims 5-6 and 8, Poisner teaches the claimed invention as described above and furthermore, Poisner teaches that once the main memory is fully configured, the stack in separate RAM is no longer needed and stack pointer is re-programmed to point to main memory (e.g. see Paragraph [0028]), i.e. the "dirty" data in the separate RAM is sent to the main memory, in other words, the temporary memory is flushed/cleared (or placed in eviction mode) by copying data from the temporary memory to the main memory as claimed.

As per claim 9, Poisner teaches the claimed invention as described above and furthermore, Poisner teaches that the main memory comprises a random access memory (i.e. the external/separate RAM for BIOS processing, the main memory 102 in Fig. 1A-1B).

As per claim 15, Poisner teaches the claimed invention as described above and furthermore, Poisner teaches that the copying of content from the temporary memory location to the main memory occurs during pre-boot (e.g. see Paragraph [0028]).

As per claims 10-13, Poisner teaches the claimed invention as described above and furthermore, Poisner teaches that once the main memory is fully configured, the stack in separate RAM is no longer needed and stack pointer is re-programmed to point to the main memory (e.g. see Paragraph [0028]). The step of calculating and applying migration factor in order to point to the main memory is inherently embedded in the step

of re-programmed stack pointer to point to the main memory taught by Poisner. Based on this rationale, claims 10-13 are rejected.

As per claims 16-17, 19-21, 23-28 and 30, see arguments with respect to the rejection of claims 1-2, 4-6, 8-13 and 15, respectively. Claims 16-17, 19-21, 23-28 and 30 are also rejected based on the same rationale as the rejection of claims 1-2, 4-6, 8-13 and 15, respectively.

As per claims 31-32, 34-36, 38-43 and 45, see arguments with respect to the rejection of claims 1-2, 4-6, 8-13 and 15, respectively. Claims 31-32, 34-36, 38-43 and 45 are also rejected based on the same rationale as the rejection of claims 1-2, 4-6, 8-13 and 15, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-4, 7, 18-19, 22, 33-34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner in view of the 'Background of Invention' section of the current application, hereinafter, BOI.

As per claim 3, Poisner teaches the claimed invention as described above but does not teach that the content of the temporary memory comprises heap data. However, BOI teaches that the content of the temporary memory (i.e. the external

memory) comprises stack and heap data (e.g. see paragraphs [0003] and [0005]). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teaching of BOI in the method taught by Poisner. In doing so, dynamically allocated data structures, i.e. storage that is not known until the program is running, can be stored temporary memory during pre-boot.

As per claim 4, Poisner teaches the claimed invention as described above and furthermore, Poisner *inherently* teaches that the temporary memory comprises a cache memory (i.e. CPU's cache memory; embedded in CPU 100 in Fig. 1A-1B) (e.g. see Paragraph [0005] and Figs. 1A-1B). Suppose if the Applicant is not agree with Examiner for this inherency feature, Examiner would like to support it by secondary reference. BOI teaches that the temporary memory comprises a cache memory (i.e. the on-board processor cache) (e.g. see paragraph [0005]).

As per claim 7, the combination of Poisner and BOI teaches the claimed invention as described above and furthermore, BOI teaches that the cache memory comprises one of (i) an L1 cache memory, and (ii) an L2 cache memory (i.e. the on-board processor cache) (e.g. see paragraph [0005]).

As per claims 18-19 and 22, see arguments with respect to the rejection of claims 3-4 and 7, respectively. Claims 18-19 and 22 are also rejected based on the same rationale as the rejection of claims 3-4 and 7, respectively.

As per claims 33-34 and 37, see arguments with respect to the rejection of claims 3-4 and 7, respectively. Claims 33-34 and 37 are also rejected based on the same rationale as the rejection of claims 3-4 and 7, respectively.

6. Claims 14, 29 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner in view of Meyer (USPN: 2002/0099909).

As per claims 14, 29 and 44, Poisner teaches the claimed invention as described above but does not teach that the value in the main memory is verified as identifying the temporary memory by determining if the value is greater than a bottom of the temporary memory and is less than a top of the temporary memory. Meyer, on other hand, teaches that the value in the main memory is verified as identifying the temporary memory by determining if the value (i.e. the address received from the processor 10 in Fig. 1) is greater than a bottom of the temporary memory and is less than a top of the temporary memory (i.e. within the main memory 100 in Fig. 1 or the low-latency memory 130 in Fig. 1; the temporary memory in this application) (e.g. see paragraph [0028] and Fig. 1). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teaching of Meyer in the method taught by Poisner so it can be determined whether to modify the value in main memory during migration before the boot process ends.

Remarks

7. As to the remark, Applicant asserted:

(a) Poisner does not describe or suggest calculating a migration factor between a temporary memory location and a main memory location. Neither the cited portions of the specification nor the figures describe calculating a migration factor between a temporary memory location and a main memory location.

(b) Since the Poisner was, at the time the claimed invention was made, owned by the same assignee (Intel Corp.), Poisner is not available as prior art for 35 USC 103 in accordance with 35 USC 103 (c).

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), Poisner does teach about calculating a migration factor between a temporary memory location and a main memory location, i.e. by re-programming the stack pointer to point to main memory (e.g. see Col. 4, lines 23-24).

With respect to (b), since the Poisner et al. (USPN: 2002/0199093) prior art is a 102(a) prior art, i.e. published before the priority date of the current application, 35 USC 103(c) cannot be used to prevent the use of Poisner et al. (USPN: 2002/0199093) prior art or 35 USC 103.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HBP
HBP

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100